Cortina Systems® LXT973 10/100 Mbps Dual-Port Fast Ethernet PHY Transceiver

Specification Update

20 March 2007

Document Number 249737

Revision 10.0

Contents

1.0 Revision History

Revision 10.0 **Revision Date: 20 March 2007**
First release of this document from Cortina Systems, Inc.

Revision: 009 **Revision Date: 29 November 2005**
Added/modified top label markings under Identification Information.
Modified Table 3, *Product Ordering Information* and Figure 4, *Ordering Information – Sample* under Documentation Changes.

Revision: 008 **Revision Date: 07 March 2005**
Added Erratum 10: Section 10, *Port 1 LED Functionality Incorrect when Port 0 in Hardware Power-Down Mode*

Revision: 007 **Revision Date: 14 May 2004**
Added Documentation Changes 2 and 3 to Section 8.0, *Documentation Changes* section.

Revision: 006 **Revision Date: 12 February 2003**
Added Errata 6 through 9 to Section 3.2, *Errata* table.
Changed status on Erratum 4: “MDIO Interface and Repeated Polling”.
Changed status on Erratum 5: “3.3 V Fiber Speed Selection”.
Added Erratum 6: “Far-End Fault Reporting” to Section 5.0, *Errata* section.
Added Erratum 7: “Internal Loopback Receive Disable” to Section 5.0, *Errata* section.
Added Erratum 8: “Changing Advertised Duplex While Link Is Up” to Section 5.0, *Errata* section.
Added Erratum 9: “Detection of Illegal Symbols After SSD” to Section 5.0, *Errata* section.

Revision: 005 **Revision Date: 03 October 2002**
Added “Establishment of Link in Forced 100 Mbps Mode”, “MDIO Interface and Repeated Polling”, and “3.3 V Fiber Speed Selection” to the Errata table.
Added Erratum 3 “Establishment of Link in Forced 100 Mbps Mode”.
Added Erratum 4 “MDIO Interface and Repeated Polling”.
Added Erratum 5 “3.3 V Fiber Speed Selection”.

Revision: 004 **Revision Date: 14 March 2002**
Modified Table 1, “Product Information”. Replaced MM numbers.

Revision: 003 **Revision Date: 01 August 2001**
Corrected Manufacturer's Revision Number in Markings table.
Added Product Ordering Information.

Revision: 002 **Revision Date: 31 May 2001**
Added Erratum #2.

Revision: 001 **Revision Date: 18 May 2001**
Added Erratum #1.

2.0 Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

2.1 Affected Documents/Related Documents

Title	Document Number
LXT973 10/100Mbps 2-Port Fast Ethernet PHY Transceiver Datasheet	249426
LXT973 Frequently Asked Questions	249708
LXD973 Development Kit Manual (Demo Board)	249719
LXD973 Design and Layout Guide	249631

2.2 Nomenclature

Errata are design defects or errors. These may cause the behavior of the Cortina Systems® LXT973 10/100 Mbps Dual-Port Fast Ethernet PHY Transceiver (LXT973 PHY Transceiver) to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

3.0 Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the LXT973 PHY Transceiver.
Cortina Systems, Inc. (Cortina) may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

3.1 Codes Used in Summary Table

3.1.1 Stepping

X: Errata exists in the stepping indicated. Specification Change, or Specification Clarification applies to this stepping.

(No mark) or (Blank box): This erratum is fixed in stepping indicated. Specification Change, or Specification Clarification does not apply to this stepping.

3.1.2 Page

(Page): Page location of item in this document.

3.1.3 Status

Doc: Document change or update will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

3.2 Errata (Sheet 1 of 2)

No.	Steppings		Page	Status	ERRATA
	1	2			
1	X	X	page 10	NoFix	Section 1, *Speed LED Stays Active During Reset*
2	X	X	page 10	NoFix	Section 2, *Delay of Link While in Auto MDI/MDIX Enabled, Forced 100 Mbps Mode*
3	X	X	page 10	NoFix	Section 3, *Establishment of Link in Forced 100 Mbps Mode*
4	X		page 11	Fixed	Section 4, *MDIO Interface and Repeated Polling*
5	X		page 11	Fixed	Section 5, *3.3 V Fiber Speed Selection*
6	X		page 11	NoFix	Section 6, *Far-End Fault Reporting*
7	X	X	page 12	NoFix	Section 7, *Internal Loopback Receive Disable*

3.2 Errata (Sheet 2 of 2)

No.	Steppings		Page	Status	ERRATA
	1	2			
8	X	X	page 12	NoFix	Section 8, *Changing Advertised Duplex While Link Is Up*
9	X	X	page 12	NoFix	Section 9, *Detection of Illegal Symbols After SSD*
10	X	X	page 13	NoFix	Section 10, *Port 1 LED Functionality Incorrect when Port 0 in Hardware Power-Down Mode*

3.3 Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	#	#			
					None for this revision of this specification update.

3.4 Specification Clarifications

No.	Steppings		Page	Status	SPECIFICATION CLARIFICATIONS
	#	#			
					None for this revision of this specification update.

3.5 Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	002	page 17	Doc	Product Ordering Informationand Figure 1, “Ordering Information - Sample”
2	003	page 19	Doc	Item 2:, *Change to Table for Port 0 Signal Descriptions*
3	003	page 19	Doc	Item 3:, *Change to Table for Port 1 Signal Descriptions*

4.0 Identification Information

4.1 Markings

Figure 2 shows a sample PQFP package for the LXT973 PHY Transceiver.

Notes:

1. In contrast to the Pb-Free (RoHS-compliant) PQFP package, the non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.
2. Further information regarding RoHS and lead-free components can be obtained from your local Cortina representative.

Figure 1 Example of Top Marking Information Labeled as Cortina Systems, Inc.

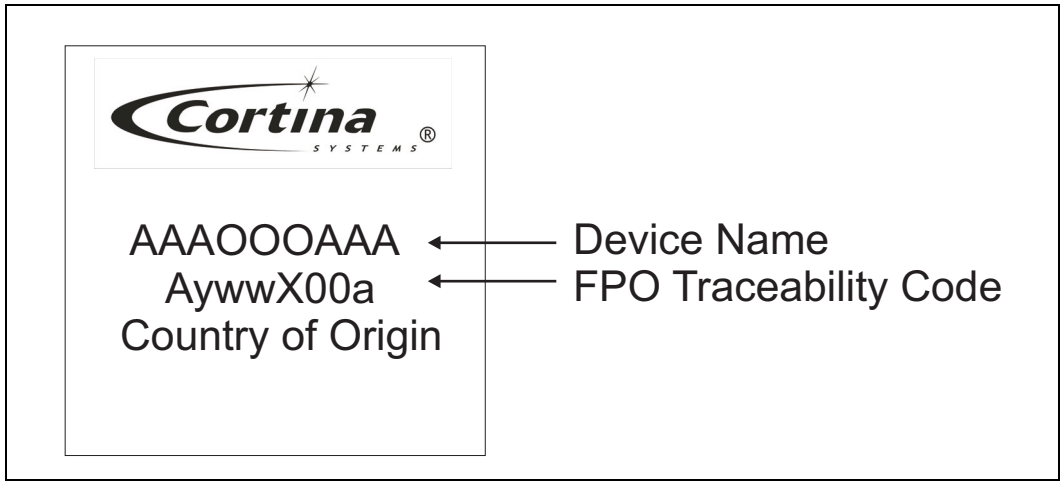


Figure 2 Sample PQFP Package – Intel* LXT973QC Transceiver

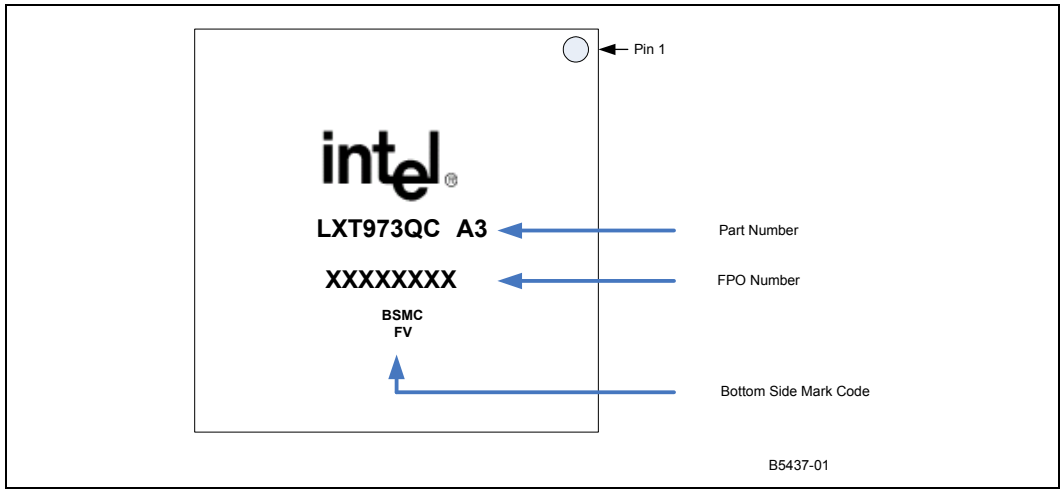
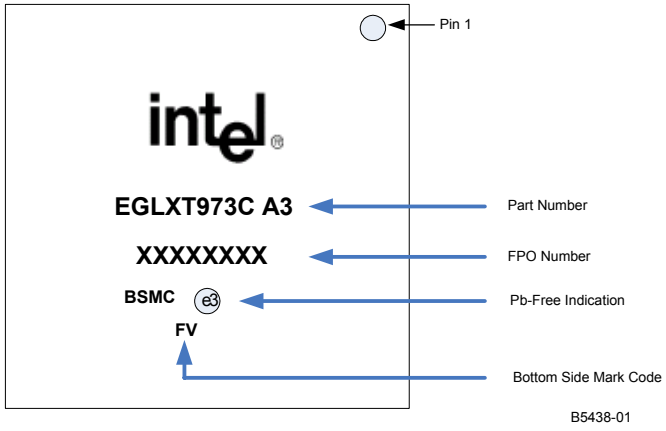


Figure 3 shows a sample Pb-free RoHS-compliant PQFP package for the LXT973 PHY Transceiver.

Figure 3 Sample Pb-Free (RoHS-Compliant) PQFP Package – Intel* EGLX973QC Transceiver



The silicon stepping in the LXT973 PHY Transceiver Datasheet is referred to as “Manufacturer’s Revision Number”. The silicon stepping revision number may be read by software from Register 3, bits 3:0 in the LXT973 PHY Transceiver.

Stepping	Revision Number	Manufacturer’s Revision Number[1]	Part Number
1	A2	0000	LXT973
2	A3	0001	LXT973

1. This value is from Register bits 3.3:0. See the LXT973 PHY Transceiver datasheet for more information.

5.0 Errata

Item 1: Speed LED Stays Active During Reset

Problem During reset, the speed LED on both ports stays lit. The other LED functions are turned off during reset. This erratum has been confirmed on all LED modes with the speed functionality display while RESET is held active. All other functions such as Link, Activity, Duplex Status, and MII Isolate turn off during reset.

Implication Monitoring the speed LED during reset may be misleading. The LED functions properly during normal operation.

Workaround None.

Status There are no plans to fix this erratum.

Item 2: Delay of Link While in Auto MDI/MDIX Enabled, Forced 100 Mbps Mode

Problem The LXT973 PHY Transceiver may have difficulty determining the MDI/MDIX setting under the following conditions:

- Forced 100 Mbps mode
- Auto MDI/MDIX is enabled
- Link partner is auto-negotiation enabled

Implication The LXT973 PHY Transceiver may take several seconds to establish link under the following conditions:

- LXT973 PHY Transceiver is forced to 100 Mbps
- Auto MDI/MDIX is enabled
- Link partner is auto-negotiation enabled

Workaround Disable auto MDI/MDIX when in forced 100 Mbps mode.

Status There are no plans to fix this erratum.

Item 3: Establishment of Link in Forced 100 Mbps Mode

Problem Link may not come up reliably when the following occurs:

- The LXT973 PHY Transceiver is in forced 100 Mbps mode and link is down.
- The link partner is configured to auto-negotiate.
- The link partner cannot handle instantaneous jitter on the MLT3 signal during link-up.

Implication If this condition occurs, communication between the LXT973 PHY Transceiver and its link partner may not establish. This condition does not occur in other speed setting combinations.

Workaround Configure the LXT973 PHY Transceiver in auto-negotiation rather than forced 100 Mbps mode, or configure the link partner to forced 100 Mbps instead of auto-negotiation to establish link.

Status There are no plans to fix this erratum.

Item 4: MDIO Interface and Repeated Polling

Problem Repeated polling of odd-numbered registers via the MDIO interface randomly returns the contents of the previous even register.

Implication Managed applications may not obtain the correct register contents when a particular register is monitored for device status.

Workaround None.

Status This erratum has been previously fixed.

Item 5: 3.3 V Fiber Speed Selection

Problem In fiber mode, the hardware configuration pins (SD_2P5V/SPEED*n*) set the speed rather than set the signal detect voltage threshold.

Implication Setting the SD_2P5V/SPEED*n* to Low sets the device in 10 Mbps operation, which is not supported in fiber mode. The signal detect function defaults to 2.5 V PECL thresholds. The signal detect input is unreliable when driven from a 3.3 V PECL source.

Workaround To select 100 Mbps operation in fiber mode, tie the SD_2P5V/SPEED*n* configuration pins High through a 10 KΩ resistor to VCC.

To properly terminate the signal detect input, tie the SD*n* pins High through a 10 KΩ resistor.

There is no workaround to enable the SD function when using a 3.3 V optical module.

Status This erratum has been previously fixed.

Item 6: Far-End Fault Reporting

Problem If a link partner continuously sends successive Far-End Fault (FEF) codes (three sets of 84 1s followed by a 0), the LXT973 PHY Transceiver sets the Remote Fault bit High (Register bit 1.4 = 1) and drops link (Register bit 1.2 = 0). Register bit 1.4 is cleared after a Read and is not set High again while the Far-End Fault signal is present.

Implication If the MAC reads Register bit 1.4 more than once under a continuous Far-End Fault condition, a Far-End Fault is not indicated after the first read.

Once a remote fault has been indicated by Register bit 1.4 = 1, the following sequence can be used to monitor the remote-fault status.

Managed Systems:

- Write Register 0 = 0x6100: Forces the port to 100 Mbps full-duplex internal loopback, link is up, Register bit 1.2 = 1 and Register bit 1.4 = 0.
- Wait: Approximately 100 mS.
- Write Register 0 = 0x2100: Forces the port into 100 Mbps full-duplex. If Far-End Fault is present, Register bit 1.4 = 1 indicates Far-End Fault and Register bit 1.2 = 0 indicates link is down.

Status This erratum has been previously fixed.

Item 7: Internal Loopback Receive Disable

Problem The recovered clock from the receive data is used instead of the transmit clock when setting a port to 10 Mbps internal loopback mode.

Implication When the port is connected to a link partner transmitting data or idle signals, the loopback data is corrupted because the receiver data recovered clock is used to capture the loopback data.

Workaround Clear Register bit 16.8 so that the proper clock is used. This bit is set on power-up.

Status There are no plans to fix this erratum.

Item 8: Changing Advertised Duplex While Link Is Up

Problem Writing to Register bits 4.9:5, which control duplex mode advertisement while link is up and auto-negotiation is enabled, immediately changes the PHY mode of operation to the new duplex mode. When written, the values in this register are not intended to affect PHY operation until a new auto-negotiation cycle is completed.

Implication A possible mixed-duplex operation will exist during the time between Register bits 4.9:5 writes and the start of a new auto-negotiation process.

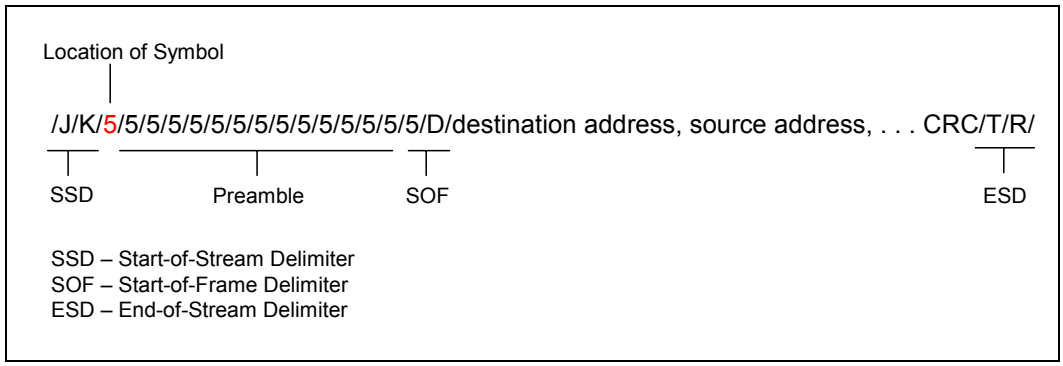
Workaround Write Register bits 4.9:5 immediately before the start of a new auto-negotiation process.

Status There are no plans to fix this erratum.

Item 9: Detection of Illegal Symbols After SSD

Problem An illegal symbol placed immediately after the Start-of-Stream Delimiter (SSD) (preamble after JK) is not detected. However, any subsequent corrupt symbol will be detected.

Standard Frame Contents:



Implication RXER will not assert if this symbol location is corrupted. However, an error in this location does not affect packet integrity.

Workaround Use the MAC layer protocol to detect corrupt symbols in the packet.

Status There are no plans to fix this erratum.

Item 10: Port 1 LED Functionality Incorrect when Port 0 in Hardware Power-Down Mode

Problem When Port 0 is placed in Hardware Power-Down mode while Port 1 is active, LED pins LED1_2 and LED1_3 do not function as specified in the table in Revision 003 of the datasheet.

Table 1 LED Configurations

LED_CFG0	LED_CFG1	LEDn_1	LEDn_2	LEDn_3
0	0	Speed	Link	Duplex
1	0	Speed	Link/Activity	Duplex/ Collision
0	1	Link	Receive	Transmit
1	1	Speed	Link/ MII Isolate	Duplex/ Collision

There are two behaviors associated with this errata.

- The blinking status of Activity, Collision, and MII Isolate are not indicated in each mode specified in the LED Configurations table. [The non-blinking status (Link or Duplex) is not affected when the LED is configured to provide dual status.]
- When only a single status is configured to be indicated (Link, Duplex, Receive, or Transmit) by LED1_2 or LED1_3, the LED stays on or off instead of switching to indicate the correct status.

Implication Monitoring LED1_2 and/or LED1_3 when Port0 is in Hardware Power-Down Mode is misleading. The following table lists the affect of the errata for each configuration.

Note: This errata affects only LEDn_2 and LEDn_3 of Port 1 only when Port 0 is in Hardware Power-Down Mode.

Table 2 LED Configurations

LED_CFG0	LED_CFG1	LEDn_1	LEDn_2	LEDn_3	Effect of Errata
0	0	Speed	Link	Duplex	Led2 and Led3 go on and stay on when Port 0 is in Hardware Power-Down mode.
1	0	Speed	Link/Activity	Duplex/Collision	Activity and Collision are ignored, and the Link and Duplex status are available and accurate.
0	1	Link	Receive	Transmit	Led2 and Led3 go off and stay off when Port 0 is in Hardware Power-Down mode.
1	1	Speed	Link/ MII Isolate	Duplex/Collision	MII isolate and Collision are ignored, and the Link and Duplex status are available and accurate.

Workaround Port 0 LEDs function properly when Port 1 is placed in Hardware Power-Down mode with the PWRDWN1 pin. As a result, depending on design requirements, the following options can be used as workarounds:

- Use Port 0 and Hardware Power-Down Port 1.

- Software Power-Down mode is not affected by this erratum. Use Register Bit 0.11 to Power-Down Port0. For design differences between Software and Hardware Power-Down Modes, see the LXT973 PHY Transceiver datasheet's Section 3.5.3, "Power-Down Mode".

Note:

- For designs that require the MII interface to be isolated, use Register Bit 0.10.
- This erratum does not affect LED1_1.

Status There are no plans to fix this erratum.

6.0 Specification Changes

There are no specification changes.

7.0 Specification Clarifications

There are no specification clarifications.

8.0 Documentation Changes

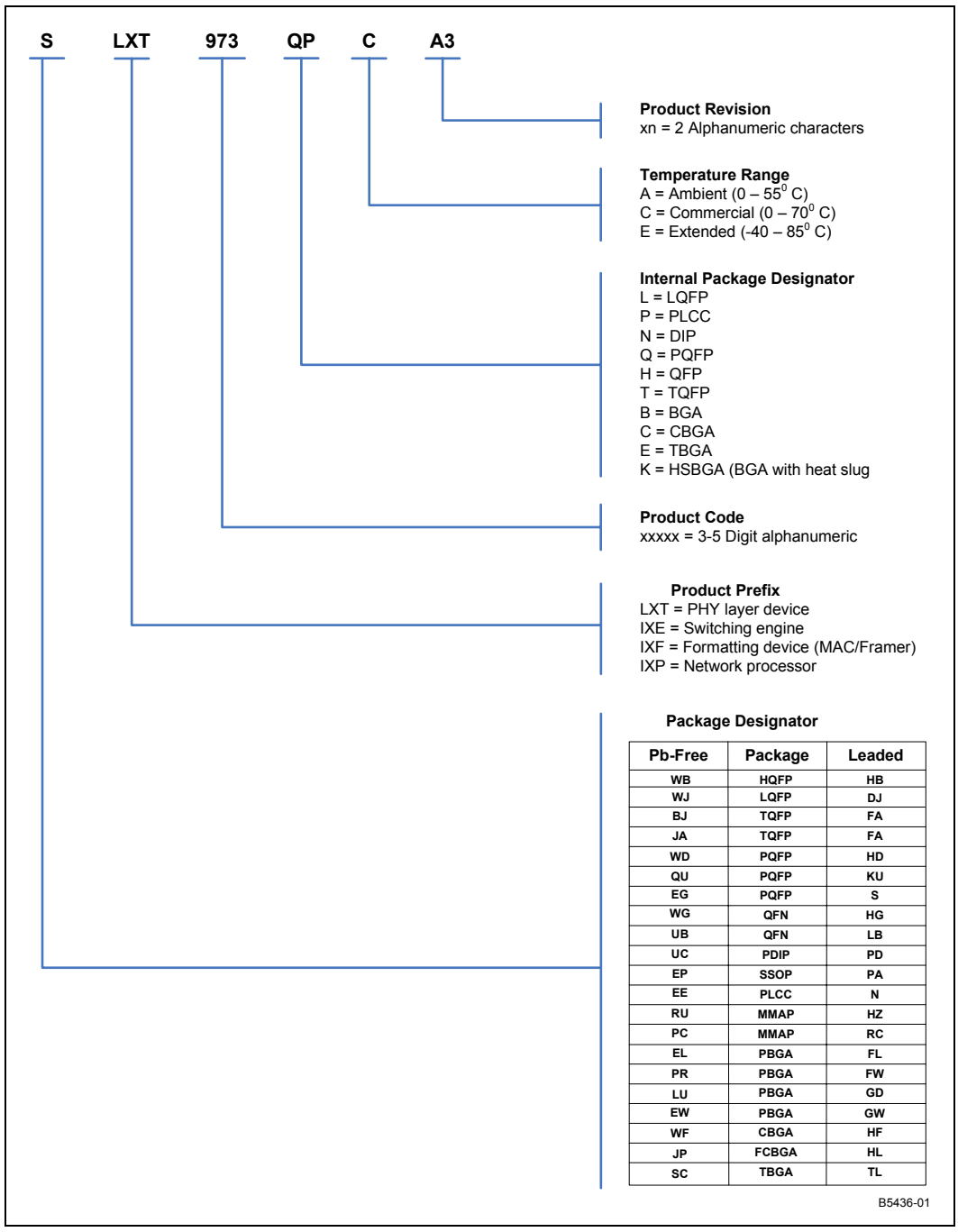
Item 1: Product Ordering Information

Table 3 lists the LXT973 PHY Transceiver product ordering information. Figure 4 provides the ordering information matrix.

Table 3 Product Ordering Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
SLXT973QC.A3V	A3	PQFP	100	No
EGLXT973QC.A3V	A3	PQFP	100	Yes
SLXT973QE.A3V	A3	PQFP	100	No
EGLXT973QE.A3V	A3	PQFP	100	Yes

Figure 4 Ordering Information – Sample



Pb-Free	Package	Leaded
WB	HQFP	HB
WJ	LQFP	DJ
BJ	TQFP	FA
JA	TQFP	FA
WD	PQFP	HD
QU	PQFP	KU
EG	PQFP	S
WG	QFN	HG
UB	QFN	LB
UC	PDIP	PD
EP	SSOP	PA
EE	PLCC	N
RU	MMAP	HZ
PC	MMAP	RC
EL	PBGA	FL
PR	PBGA	FW
LU	PBGA	GD
EW	PBGA	GW
WF	CBGA	HF
JP	FCBGA	HL
SC	TBGA	TL

Item 2: Change to Table for Port 0 Signal Descriptions

Table 4 Port 0 Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
20	MDDIS0	I	**OLD Information in table -** **Management Disable**. When MDDIS0 is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS0 is pulled Low at power-up or reset via the internal pull-down resistor or by tying it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
20	MDDIS0	I	**UPDATED Information in table -** **Management Disable**. When MDDIS0 is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS0 is pulled low at power-up or reset via an external pull-down resistor, the Hardware Control Interface Pins control only the initial values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Item 3: Change to Table for Port 1 Signal Descriptions

Table 5 Port 1 Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
19	MDDIS1	I	**OLD Information in table -** **Management Disable**. When MDDIS is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS is pulled Low at power-up or reset via the internal pull-down resistor or by tying it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
19	MDDIS1	I	**UPDATED Information in table -** **Management Disable**. When MDDIS1 is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS1 is pulled low at power-up or reset via an external pull-down resistor, the Hardware Control Interface Pins control only the initial values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

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End of Document